Edge Intelligence Computing: A RISC-V Based Ubuntu SBC System with Hardware Acceleration Capabilities

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***Abstract*-The exponential rise of edge computing necessitates robust, power-efficient, and open hardware platforms capable of supporting AI inference, 3D & Video processing, and general-purpose computing within constrained environments. Whereas x86 and ARM architectures dominate this space, they introduce licensing, cost, and security barriers. In contrast, the RISC-V64 architecture promises a truly open and modular alternative, but its adoption in real-world, application-ready edge systems remains limited due to several critical challenges: lack of mature software stacks, inadequate hardware acceleration support, and minimal integration with mainstream desktop environments.**

This paper introduces a RISC-V based Single Board Computer (SBC) running a fully operational Ubuntu 22.04 Linux distribution, architected specifically for edge intelligence workloads. A key innovation is the support for the GNOME-Wayland Window Manager, fully optimized for RISC-V with hardware acceleration via Mesa and OpenGL-ES & Vulkan-compatible drivers and GPU offloading. We demonstrate seamless execution of complex open-source desktop applications such as Mozilla Firefox, LibreOffice, MPV Media Player (4K playback with real-time hardware Video decoding), and Geney & Jupyter Web IDE, all running natively on the RISC-V64 Ubuntu 22.04 SBC. This paper demonstrates the feasibility of RISC-V as a high-performance edge computing architecture. The proposed system effectively bridges the usability gap in RISC-V-based environments but also demonstrates a scalable path for mass adoption in open-source driven, hardware-accelerated edge intelligence platforms.

Keywords - Open Instruction Set Architecture, RISC-V, Ubuntu, Hardware, Acceleration, GNOME.

I. INTRODUCTION

Open-source hardware is increasingly being recognized as a transformative force in computing, complementing the revolution initiated by open-source software such as the Linux operating system. Open Instruction Set Architectures (ISAs) provide a disruptive opportunity in the processor design space, enabling architects to build custom microarchitectures without the licensing restrictions imposed by proprietary ISAs. Among these initiatives, RISC-V has emerged as the most prominent and widely adopted open ISA, with the potential to redefine both academic research and industrial processor development, and now in Edge Computing.

Our expertise in incorporating embedded Linux systems for the RV64GC variant, leveraging open-source toolchains and build methodologies derived from Linux from the Scratch, revealed a critical gap in the availability of a desktop-grade Ubuntu distribution tailored for RISC-V64, equivalent maturity and documentation for Ubuntu on RISC-V64, with a fully functional Windowing Graphical User Stack remaining sparse. This absence of a fully optimized Ubuntu environment underscored the complexity of enabling a distribution that not only boots but also delivers a functional GNOME (Wayland) graphical stack with hardware acceleration. This standardized design allows RV64GC to serve as the reference hardware profile for modern RISC-V SBCs, ensuring compatibility with existing compilers, toolchains, and application frameworks while delivering the computational robustness required for 3D graphics acceleration, video decoding, and computer vision workloads in edge and desktop-class environments, with cost-effectiveness and improved energy efficiency, and with excellent performance characteristics for usability.

Searching for an existing Linux distribution targeting the RV64GC profile revealed a critical gap, while the Ubuntu/RISC-V project provides partial support for RV64GC, equivalent efforts for Ubuntu were either fragmented or undocumented. The lack of comprehensive resources and prior work, particularly in the context of enabling a modern Ubuntu Stack with GNOME-Wayland windowing system, posed a significant barrier to advancing Ubuntu on RISC-V. No end-to-end guides existed for building Ubuntu from scratch on RV64GC with functional integration of hardware acceleration subsystems. Recognizing this limitation, we embarked on the ambitious task of creating a fully operational Ubuntu 22.04 distribution for RISC-V64, specifically tailored to exploit GPU pipelines for enabling Hardware Acceleration for Graphical Windowing and other 3rd Party UI applications, VPU codecs, DRM/KMS display frameworks, and Vision-AI accelerators. The goal was not only to achieve kernel-level booting, but also to deliver a desktop-class environment with smooth rendering, responsive compositing, and hardware-assisted multimedia performance.

This paper presents the design, implementation, and comprehensive validation of a RISC-V64 based Single Board Computer (SBC) capable of running a full-fledged Ubuntu 22.04 graphical desktop environment. The proposed system is realized as an Ubuntu-capable RISC-V System-on-Chip (SoC), constructed using a combination of open-source building blocks and internally developed Intellectual Property (IP) components to ensure extensibility, performance, and compliance with the RV64GC profile. Key contributions include the enablement of GNOME-Wayland desktop support, hardware-accelerated graphics pipelines, and optimized multimedia subsystems necessary for modern Ubuntu Desktop workloads. By incorporating dedicated GPU and VPU acceleration, the system achieves responsive Mozilla Firefox web browsing with Video Streaming capabilities, Smooth 4K video playback in MPV, and efficient execution of productivity applications such as LibreOffice, Media Photo Editors, and GNOME-Apps. Furthermore, hardware-assisted compute paths enable computer vision and AI workloads, ensuring the platform is suitable not only for general-purpose computing but also for edge intelligence applications.

Through extensive engineering, validation, and system integration, we have successfully developed an Ubuntu 22.04 distribution explicitly targeted for the RISC-V64. This work addresses a longstanding gap in the ecosystem: the absence of a maintainable and scalable Ubuntu distribution for RISC-V64 that can support GNOME-Wayland compositing, Mesa-based GPU acceleration, and VPU-assisted multimedia decoding. Our contributions extend beyond basic kernel and user-space enablement to the complete integration of Ubuntu's package management infrastructure for riscv64, and driver stacks, ensuring long-term maintainability and reproducibility, In particular, our development pipeline validated the execution of critical open-source applications such as Mozilla Firefox for hardware-accelerated browsing and WebGL content, MPV Media Player for smooth 4K video playback leveraging VPU offload, and productivity workloads on LibreOffice and development IDEs. Each of these applications was tested within a hardware-accelerated GNOME-Wayland session, highlighting the viability of Ubuntu on RISC-V SBCs as an edge intelligence platform. By sharing our research and deployment process, we aim to provide a reproducible framework that will accelerate future adoption of RISC-V for both embedded and desktop environments, thereby strengthening the open hardware ecosystem globally.

II. RISC-V SoC ARCHITECTURE

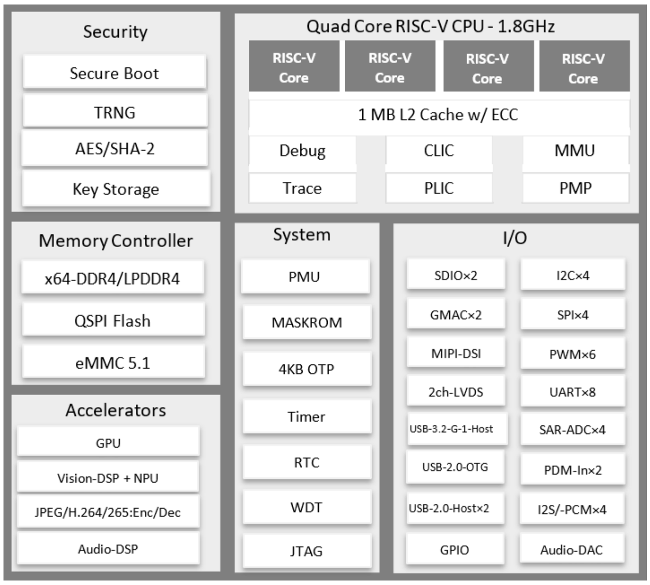

Figure 1. RISC-V SoC Architectural Block

The chip leverages an open-source System-on-Chip (SoC) platform, based on the SiFive U740 RISC-V quad-core complex, an RV64GC-class processor designed for Linux-capable, high-performance edge computing.

a) Chip Overview

The RISC-V64 SoC is a Linux-capable U74 Quad Core RISC-V processor cluster implementing the RV64GC ISA profile, optimized for high-performance embedded and edge computing. Each U74 Core is a 64-bit, dual-issue, out-of-order superscalar CPU with a 9-stage pipeline, supporting branch prediction, non-blocking load/store, and precise exception handling. The memory hierarchy comprises private L1 caches per core (32 KB I-cache, 32 KB D-cache) backed by a shared 1 MB L2 cache with coherence maintained across the cluster. The U740 implements an Sv39 MMU for 64-bit virtual memory, enabling execution of full Linux distributions such as Ubuntu 22.04, and is capable of Hardware Acceleration support.

b) Low-Power Open IP with Software Readiness

Unlike proprietary SBCs such as Raspberry Pi, which depend on closed Broadcom SoCs, our SBCs based on the RISC-V64 SoC platform prioritized openness across CPU design, SoC integration, board schematics, drivers, and firmware. While certain foundry-dependent IPs (e.g., SRAM macros, high-speed PHYs, or complex accelerators, GPU, AI, Display, Audio, VPU) remain proprietary, the overarching objective is to minimize closed components in successive iterations. This approach enables a progressively open, auditable, and Linux-capable RISC-V SBC ecosystem, advancing both research and production-grade deployments. A primary objective of the RISC-V SoC ecosystem is to deliver open-source, industrial-grade hardware IP capable of rivalling proprietary ISAs. Efforts focus on high-quality silicon implementations using rigorously verified open IP blocks, validated through real tape-out processes to meet industry standards. Crucially, openness does not compromise reliability or performance at low cost; instead, the initiative emphasizes transparent verification methodologies, fostering trust, reproducibility, and long-term scalability within the RISC-V hardware ecosystem.

c) *Domain-Specific Architectures (DSA)*

The integration of Domain-Specific Architectures (DSA) into our RISC-V64-based SoC represents a critical advancement in addressing the inherent performance and efficiency limitations of general-purpose CPU execution. While the RISC-V64 SoC core provides robust RV64GC compliance for baseline compute workloads, modern edge computing demands heterogeneous acceleration to sustain real-time performance in graphics, multimedia, Compute Vision, and Machine Learning domains.

The GPU serves as a programmable graphics and compute engine, offering full hardware acceleration for GNOME-Wayland compositing, OpenGL ES rendering, and parallelized compute workloads. This offloads complex rasterization, shading, and windowing tasks from the CPU, directly addressing the bottlenecks in GUI responsiveness and multi-application rendering on Ubuntu. Complementing this, the VPU provides dedicated H.264/H.265/VP9 decode and encode pipelines, enabling power-efficient real-time 4K video playback and adaptive streaming within applications such as MPV Media Player and Firefox. By bypassing CPU-driven software decode, the VPU ensures deterministic latency and significantly reduces memory bandwidth contention during high-bitrate multimedia workloads. For vision-centric and AI-driven applications, the Vision DSP integrates advanced SIMD units and neural network acceleration kernels optimized for convolutional layers, object detection, and inference workloads. This block empowers edge intelligence scenarios such as real-time computer vision, low-latency video analytics, and AI-assisted user interfaces, which would otherwise saturate CPU and GPU resources.

d) *Scope of Performance Improvement Solution*

The Modern RISC-V SoC developed SBCs face critical challenges, including limited CPU throughput, immature GPU/VPU driver support, and suboptimal performance for desktop-class applications. These bottlenecks hinder the poor execution of GNOME-Wayland, high-resolution video playback, and AI/Computer Vision workloads. By integrating Domain-Specific Hardware Accelerators (DSAs) comprising programmable GPUs, VPUs, and Vision-AI cores, compute-intensive tasks are offloaded from the CPU. This approach optimizes memory bandwidth, reduces latency, and enhances energy efficiency, enabling SBCs developed with RISC-V SoC to achieve near-native performance for multimedia, AI inference, and general-purpose applications while maintaining open-source flexibility, scalability, Higher Performance, Lower Power Consumption, & Higher Integration, which is the primary focus solution of RISC-V64 SoC.

e) *RISC-V Ecosystem & Community*

The RISC-V ecosystem encompasses open-source projects, commercial implementations, and global research initiatives, coordinated under the RISC-V International Foundation. Open-source cores and toolchains accelerate hardware and software innovation, while commercial products enable production-grade deployments across SBCs, SoCs, and embedded systems. Concurrently, research and educational programs drive ISA adoption, fostering experimentation, verification, and novel architectural extensions, collectively sustaining a robust, scalable, and collaborative RISC-V community.

III. RELATED WORK

Our research on RISC-V64 based edge computing has primarily addressed three dimensions: operating system enablement, graphics acceleration, and desktop environment support. Early Linux ports, including Debian and Fedora, established fundamental ISA compatibility but lacked integration with full desktop stacks or hardware offloading mechanisms. Preliminary Ubuntu efforts extended coverage but were restricted to CLI or rudimentary graphical shells without GPU/VPU acceleration. These limitations highlight the critical need for domain-specific hardware acceleration and optimized software frameworks to enable performant GNOME-Wayland desktops, 4K multimedia playback, and AI-driven workloads on RISC-V SBCs.

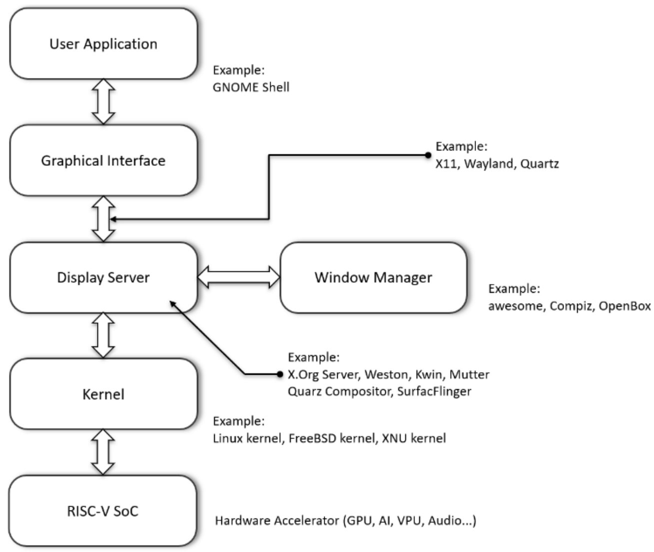

Figure 2. Software Stack Overview for Ubuntu Graphical Interface

Graphics acceleration with RISC-V SoC has been explored through frameworks like Mesa 3D, X/Wayland Server, but prior implementations faced critical shortcomings. Most relied on software rasterization (LLVMpipe), resulting in excessive CPU utilization, high memory overhead, and poor responsiveness. Attempts to enable OpenGL/ES provided only partial functionality, often limited to headless or X11-based contexts, without integration into modern compositors. Consequently, no prior work achieved full compatibility with GNOME-Wayland, where hardware-based compositing, DRM/KMS buffer management, and low-latency rendering are essential. Equally, GPU acceleration was rarely paired with VPU offload, leaving 4K video playback and multimedia applications (e.g., MPV Media Player, Firefox) constrained to inefficient software paths. This restricted both desktop usability and the execution of AI and computer vision workloads that depend on heterogeneous acceleration. To date, no implementation has delivered a fully hardware-accelerated Ubuntu desktop on RISC-V SBCs.

Desktop environment enablement on RISC-V has historically been limited by the absence of hardware acceleration. Prior efforts relied on CPU-only or Framebuffer-based rendering within lightweight window managers, which, while functional, lacked the performance to sustain complex applications. Experimental Wayland protocol implementations existed, but without GPU offload, they suffered from high latency, poor frame rates, and an inability to support productivity software or multimedia workloads. Consequently, essential use cases such as Firefox browsing, LibreOffice productivity, Shotwell, Ubuntu applications from the package managers, and 4K media playback remained impractical, underscoring the need for a fully hardware-accelerated GNOME-Wayland stack on RISC-V64. This is a gap that is identified with the right problem statement and is directly addressed by our work.

Our work closes critical gaps in RISC-V graphics enablement by:

1. Constructing a complete Ubuntu 22.04 distribution via debootstrap.
2. Embedding hardware-accelerated Mesa drivers for native GPU offloading.
3. Optimizing GNOME-Wayland with RISC-V–specific configurations.
4. Unlike prior efforts limited to software rendering or partial OpenGL/ES support, our co-designed stack from bootloader to compositor enables seamless execution of Firefox, LibreOffice, IDEs, and 4K media playback, establishing the first reproducible, desktop-grade edge intelligence platform on RISC-V64 SBCs.

IV. IMPLEMENTATION ON RISC-V64

Our implementation resolves limitations in prior RISC-V edge platforms through a three-layered design. At the OS foundation, we built Ubuntu 22.04 from RISCV ports for RV64GC distribution using *debootstrap*, generating a portable root filesystem independent of board-specific BSPs. This ensures ABI stability, upstream package compatibility, and reproducibility across heterogeneous RISC-V hardware. On this basis, we integrated GPU/VPU hardware acceleration for GNOME-Wayland compositing, OpenGL/Mesa rendering, and 4K video pipelines. Finally, we optimized critical applications Firefox, LibreOffice, MPV, and IDEs, achieving desktop-class responsiveness and enabling real-time edge AI workloads on RISC-V SoC.

a) Hardware Acceleration Integration

We enabled hardware acceleration by integrating Mesa 3D with Gallium drivers to enable the support for GPU Acceleration, DRM/KMS pipelines, and VPU offload units to support GNOME-Wayland compositing, OpenGL/ES rendering, and 4K video playback. Hardware codecs were mapped through VA-API/V4L2 backends, minimizing CPU-bound rasterization and ensuring low-latency graphics. Vectorized RISC-V extensions and FPGA overlays were configured for parallel compute workloads, bridging AI inference, real-time vision, and multimedia pipelines. This approach eliminates reliance on software-only rendering (LLVMpipe) and provides a reproducible foundation for heterogeneous acceleration across RISC-V64-based SBCs.

b) Application Optimization

On the accelerated Ubuntu stack, we optimized Firefox for GPU compositing and WebGL rendering, enabling hardware-assisted browsing performance. MPV Media Player was tuned for VPU decoding to achieve smooth 4K playback with reduced frame loss and thermal load. LibreOffice and programming IDEs were recompiled with RISC-V64 GCC/LLVM toolchains, leveraging compressed and floating-point (F/D) extensions with optimised compiler flags. Edge AI workloads (e.g., TensorFlow Lite, OpenCV) were mapped to vector extensions and SoC hardware accelerators, ensuring real-time inference performance while preserving compatibility with Ubuntu's package management ecosystem.

c) Ubuntu Windowing System Overview on RISC-V64 SoC.

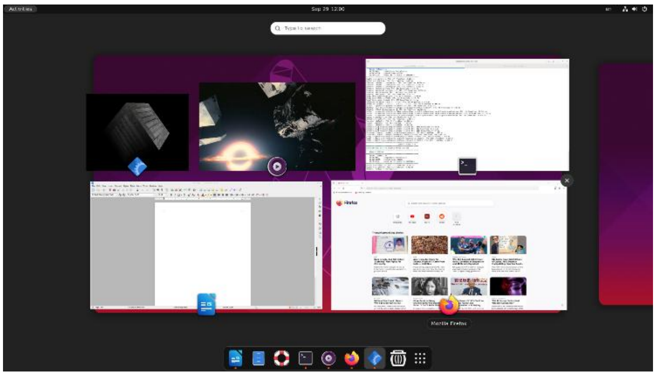

Figure 3. Hardware Acceleration Enabled RISC-V64 with Ubuntu 22.04

The GNOME-Wayland desktop on Ubuntu 22.04 RISC-V64 demonstrates concurrent execution of GLMark2-ES2 Benchmark, Mozilla Firefox, MPV Media Application, and LibreOffice, validating full-stack enabled for hardware acceleration. This showcases seamless Hardware integration (with Multimedia subsystems), stable compositor performance, and optimized application responsiveness, establishing the RISC-V64 System as viable for real-world productivity, multimedia, and graphics-intensive workloads and suitable for SBCs or High-Performance Computing.

V. RESULTS & SYSTEM INTEGRITY TESTS

To validate the RISC-V64 SoC System Stability & Integrity of Ubuntu 22.04 on the RISC-V SoC, we conducted extensive kernel, driver, and user-space testing across:

a) Application & Stability Tests:

- GNOME-Wayland, Mesa GPU pipelines, and VPU-accelerated multimedia frameworks. Core applications, including GLMark2-ES2, Firefox, LibreOffice, MPV Media Player, and IDE toolchains, were benchmarked under real-world workloads such as hardware-accelerated 4K video playback, WebGL rendering, and computer vision inference, and real-time camera streaming via the Network.

b) Extensive Workload & Continuous Operation Test:

- The system demonstrated consistent workload compatibility, low compositor latency, and sustained performance under stress conditions for over 30 continuous days, even under maximum GPU Utilisation. The Thermal, Memory & CPU utilisation were continuously monitored, and the system state was nominal, confirming the viability of Ubuntu 22.04 distribution on RISC-V SoC as a stable, hardware-accelerated platform for both edge intelligence computing and desktop-class deployments.

VI. PERFORMANCE EVALUATION

Ubuntu 22.04 on RISC-V SoC was validated using Dhrystone, CoreMark, and GLMark2-ES2, ensuring ISA correctness, benchmarking compute throughput, and confirming GPU acceleration under GNOME-Wayland, thereby demonstrating functional integrity and performance viability for edge intelligence and desktop-class workloads.

a) CPU Benchmark Results:

Benchmarking with CoreMark and Dhrystone demonstrates that RISC-V64 SoC achieves superior instruction throughput and computational efficiency compared to the i.MX8 Cortex-A53, validating its architectural advantages in pipeline efficiency, memory access patterns, and ISA extensibility, establishes RISC-V as a more performant foundation for edge intelligence workloads.

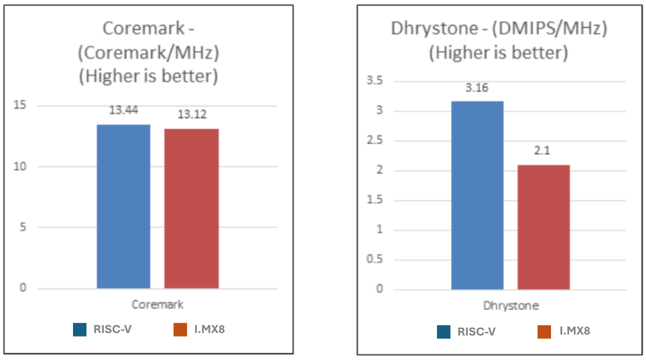

Figure 4. CPU Benchmark Comparison

b) GPU Performance Benchmark Results:

GLMark2-ES2 under GNOME-Wayland reveals that RISC-V64 outperforms the Vision-Five2, a RISC-V64 platform, delivering higher frame rates, improved execution, and lower compositor latency. These results confirm the effectiveness of the GPU acceleration pipeline and memory bandwidth utilization on Ubuntu 22.04, establishing it as a superior platform for graphics-intensive edge intelligence workloads.

Figure 5. GLMark2-ES2-Wayland Benchmark on Ubuntu 22.04 with RISC-V64 SoC

c) Object Detection & Image Classification Results on RISC-V64 with GPU Acceleration:

On an RISC-V64 System with Ubuntu 22.04, we evaluated the performance of MobileNetSSD, SqueezeNetSSD, YOLOv7, YOLOv8, and YOLOv11 using the Vulkan-NCNN framework with a GPU-accelerated platform. Results highlight efficient execution across both lightweight and compute-intensive CNN workloads, achieving real-time object detection performance. These findings confirm that the RISC-V64 ecosystem with Ubuntu provides a scalable, production-ready foundation for deploying advanced edge AI applications, bridging the gap between open ISA flexibility and high-performance deep learning inference at the edge.

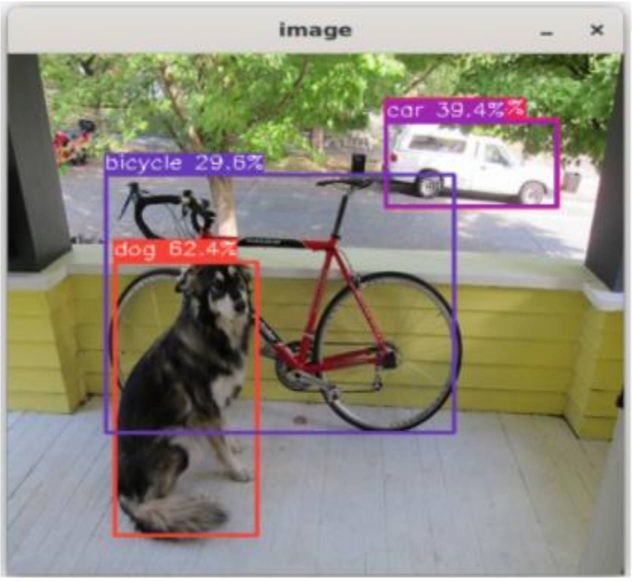

Figure 6. Object Detection Via GPU

Figure 7. Image Classification (Vehicles) Via GPU

Table 1. Computing NCNN framework on RISC-V64 vs VisionFive2 SoC for GPU on Ubuntu 22.04

Model Name	**Source File**	**U74 RISCV CPU - Inference Time (sec)**	**VF2 - Inference Time (sec)**	**RISC-V with GPU - Inference Time (sec)**
MobileNetSS		5.213	1.817	1.121
SqueezeNetSSD	Image – Vehicles	4.787	1.225	1.014
Yolov7		4.547	4.410	1.217
Yolov8		3.255	2.445	0.871
Yolov11		2.328	2.632	0.667

5. CONCLUSION

This work demonstrates that RISC-V64 SoC, when integrated with Ubuntu 22.04 and hardware acceleration frameworks, offers a practical and technically robust foundation for edge intelligence computing. The open-hardware ISA eliminates licensing costs, enabling cost-efficient customization of microarchitectures for domain-specific workloads such as real-time inference, secure IoT, and embedded intelligence HPC. Benchmarks reveal that RISC-V SoC with Hardware acceleration achieves superior performance-per-watt compared to ARM Cortex-A53, VisionFive2, a RISC-V based SBC, and competitive efficiency against x86 SBCs, while maintaining scalability from lightweight embedded systems to high-throughput edge servers.

RISC-V's modular ISA extensions (vector, crypto, DSP) combined with Ubuntu 22.04 Window System software stacks (Mesa, Vulkan-NCNN, GNOME-Wayland integration) deliver end-to-end acceleration, addressing prior limitations in graphics, AI inference, video processing, and desktop-class computing on open ISAs. Furthermore, the ecosystem supports maintainability and longevity, as open toolchains (LLVM/GCC) and community-driven kernel support reduce vendor lock-in and accelerate innovation. The convergence of open ISA flexibility, cost efficiency, and scalable performance positions RISC-V64 SoC as a credible alternative to ARM and x86 in edge intelligence, SBCs, and specialized accelerators. This establishes RISC-V not only as a research platform but as a deployable, production-ready architecture for the next generation of domain-specific, power-efficient computing at the edge.

VII. FUTURE WORK

Future efforts will focus on deep optimization of the window system acceleration stack for RISC-V64 SoC, particularly targeting Ubuntu 24.04 for the Windowing System focused on GNOME-Wayland. By enhancing GPU/VPU driver maturity, compositor offloading, and Vulkan/Mesa integration for Xorg & Wayland Window Systems, we aim to achieve real-time, low-latency rendering for both desktop-class workloads, compute-intensive, and media visualization tasks. This optimization will directly improve performance in 4K video playback, computer vision, and scientific visualization, enabling researchers and developers to harness RISC-V64 hardware for advanced computational domains. Parallel work will involve extending the Ubuntu 22.04/24.04 Server editions into a scalable HPC framework optimized for RISC-V64 SoCs. Efforts include leveraging cluster-aware schedulers, RISC-V vector extensions (RVV 1.0), and accelerated AI frameworks to unlock high-throughput, power-efficient execution for data-intensive applications.

Collaboration with RISC-V International, Ubuntu, GNOME, Linux Kernel, and other open-source communities will be key to upstreaming enhancements, ensuring sustainability, maintainability, and long-term ecosystem adoption. Beyond graphics and HPC, future directions will include enhanced security extensions, memory bandwidth optimizations, and domain-specific accelerators for AI/ML, cryptography, and edge inference.

By aligning open-source software innovation with open ISA hardware advancements, this initiative seeks to democratize high-performance computing, positioning RISC-V64 SoC as a cornerstone architecture for scalable, accessible, and domain-optimized edge intelligence computing.

VIII. REFERENCES

[1] A Survey of RISC-V CPU for IoT Applications

[2] Chapter 10: Architectural trends in RISC-V, GPUs, TPUs, and domain-specific artificial intelligence accelerators

[3] Advanced Embedded System Modelling and Simulation in an Open-Source RISC-V Virtual Prototype

[4] Ramping Up Open-Source RISC-V Cores: Assessing the Energy Efficiency of Superscalar, Out-of-Order Execution

[5] A “New Ara” for Vector Computing: An Open Source Highly Efficient RISC-V V 1.0 Vector Processor Design

[6] Development of Fedora Linux Distribution for RISC-V (RV64G) Architecture

[7] An Academic RISC-V Silicon Implementation Based on Open-Source Components

[8] Building an Open-Source Linux Computing System On RISC-V

[9] An experimental comparison of RISC-V processors: performance, power, area, and security

[10] Survey of Verification of RISC-V Processors

[11] A Comparative Survey of Open-Source Application-Class RISC-V Processor Implementations